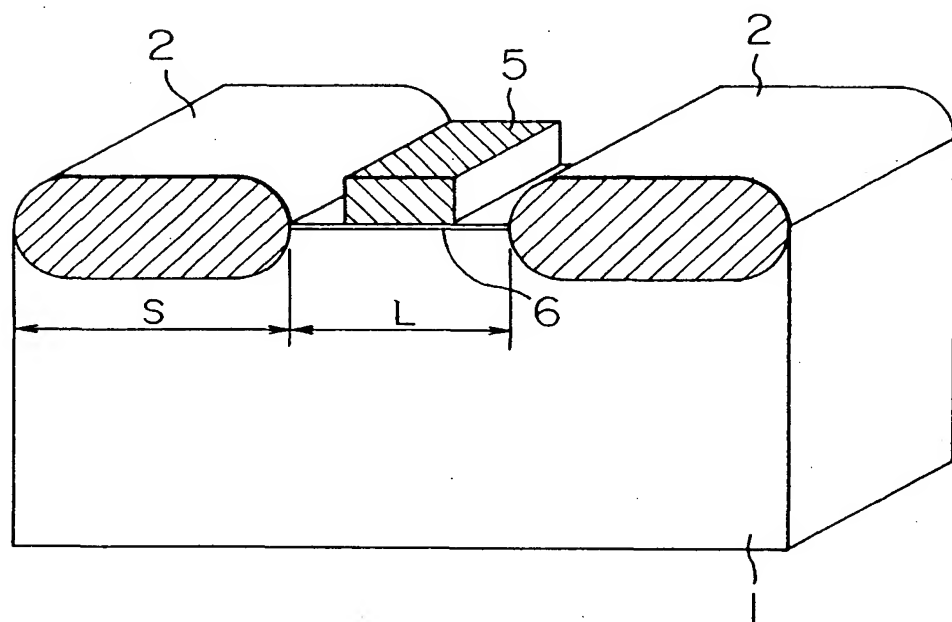


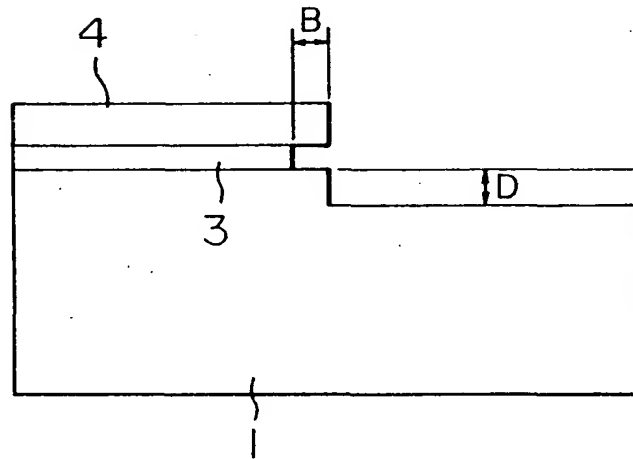
**FIG. 1**

THREE-DIMENSIONAL LOCOS SHAPE

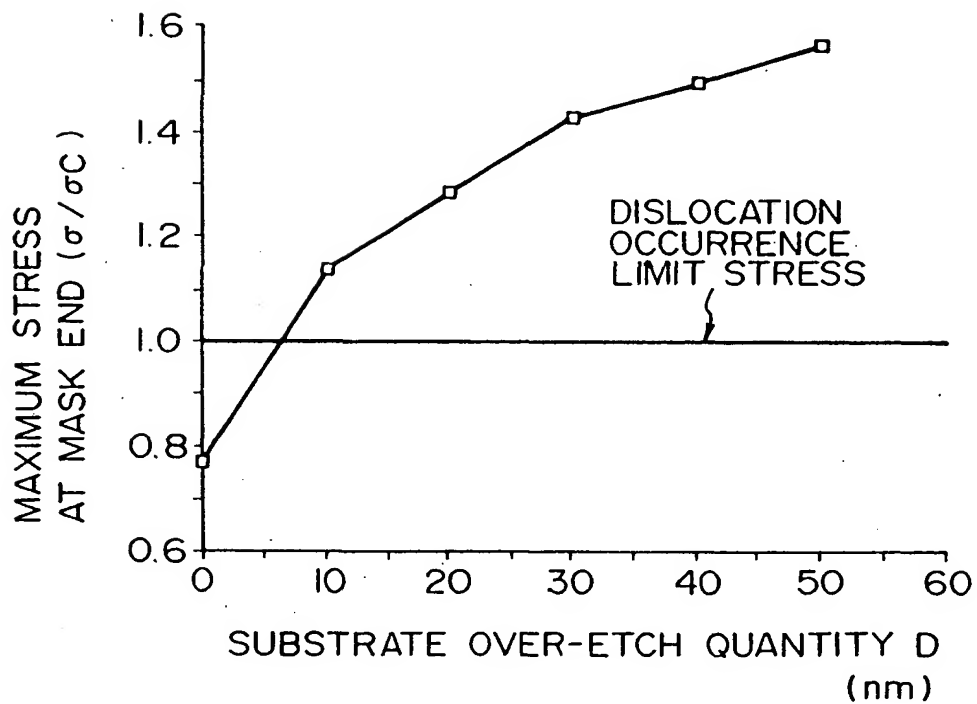


**FIG. 2A**

EXAMPLE OF ANALYSIS OF STRESS INCREASING CONDITION  
AT THE TIME OF FORMATION OF GROOVE

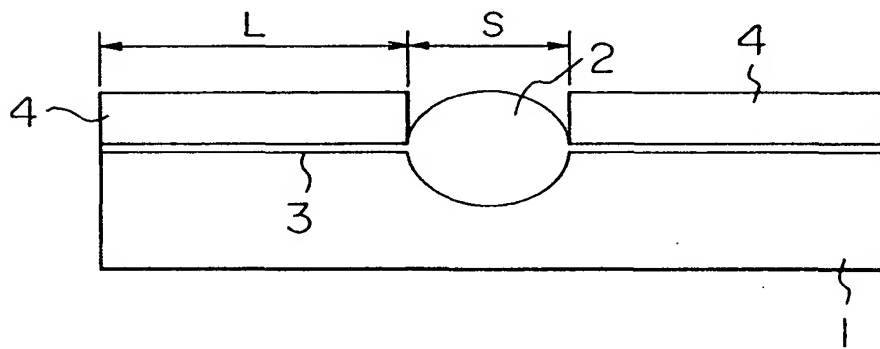


**FIG. 2B**

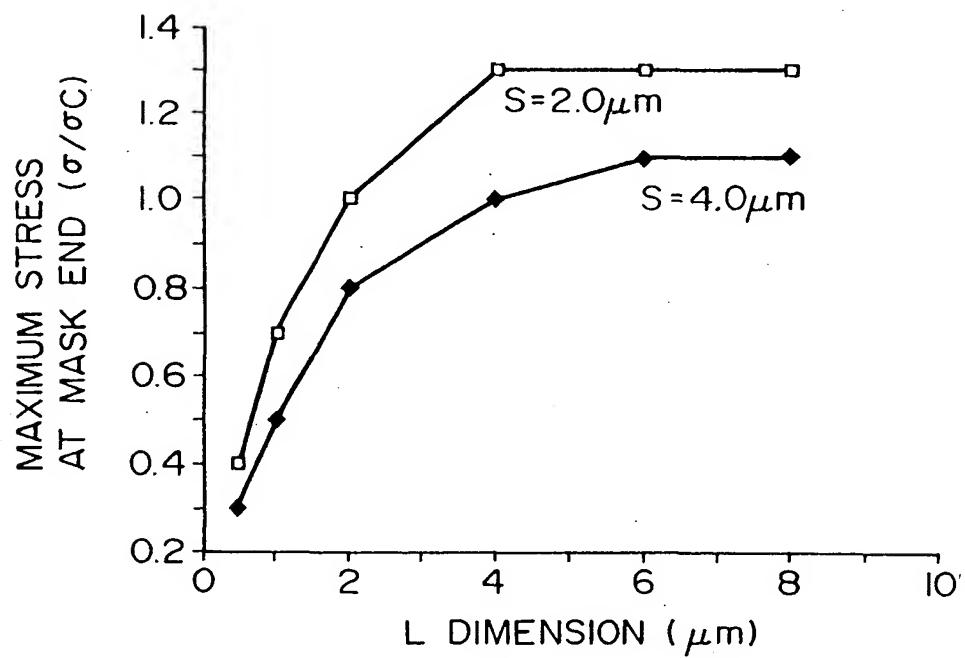


**FIG. 3A**

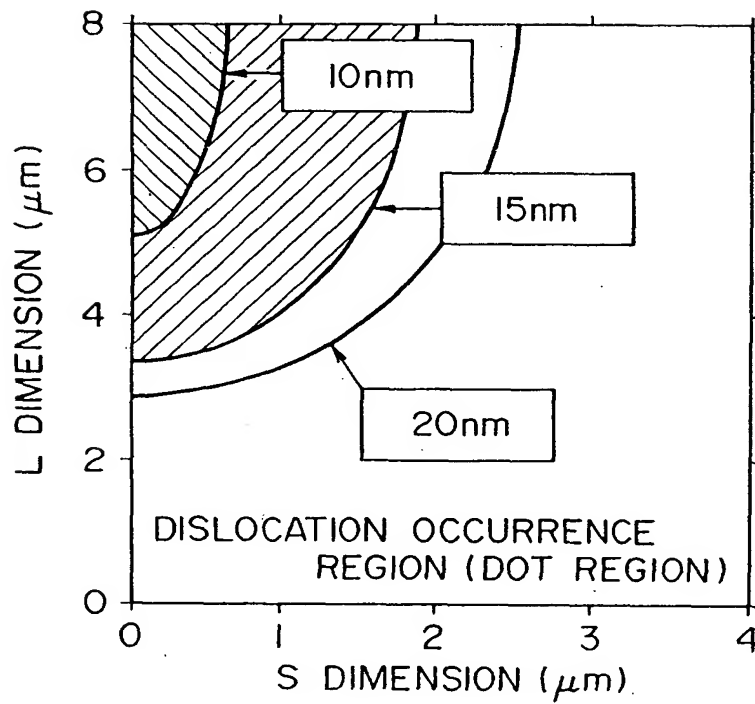
EXAMPLE OF ANALYSIS SHOWING DEPENDENCE  
OF RESULTING STRESS ON L/S DIMENSION



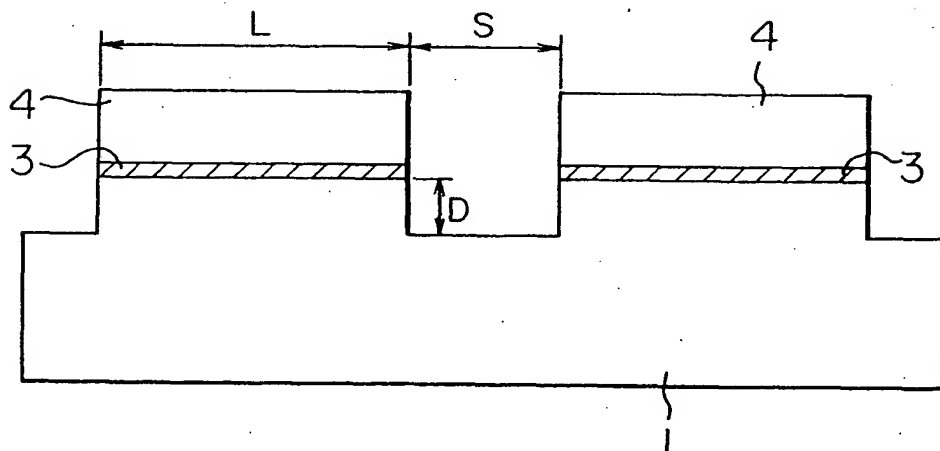
**FIG. 3B**



**FIG. 4**  
EXAMPLE OF DESIGN CHART

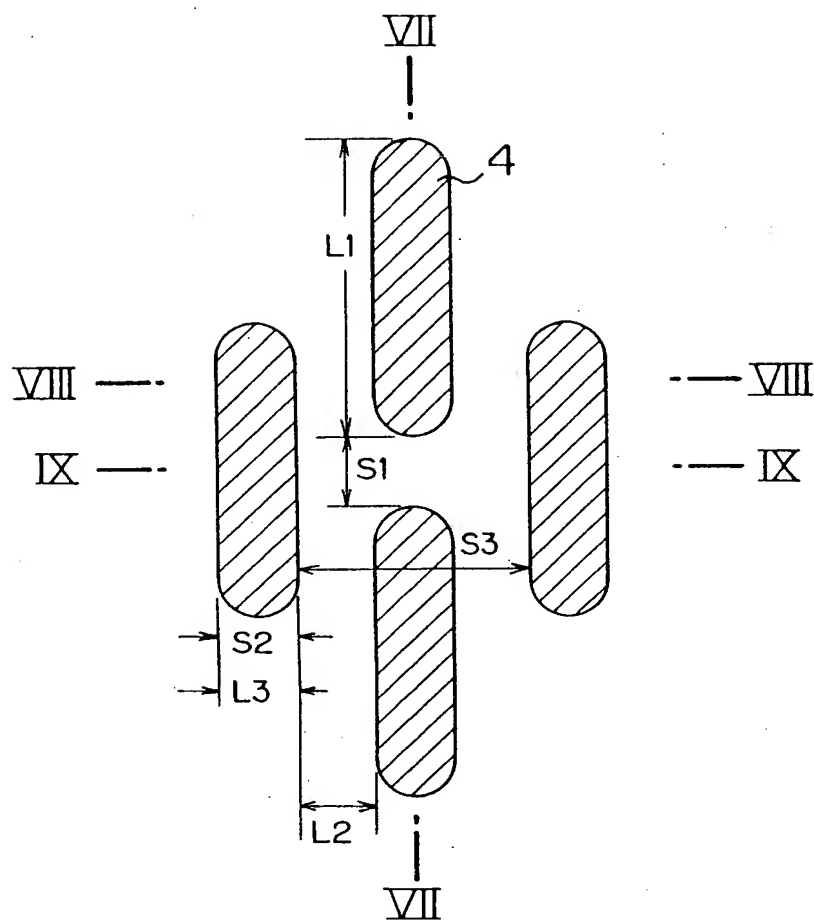


**FIG. 5**  
SECTIONAL VIEW IN DEVICE ISOLATION STEP



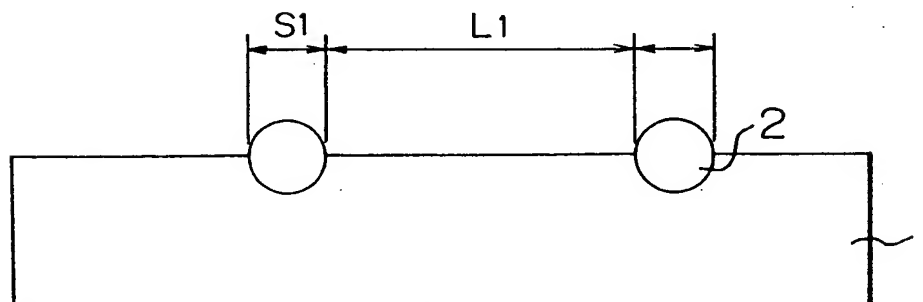
**FIG. 6**

PLAN VIEW WHEN FORMING DEVICE ISOLATION REGION



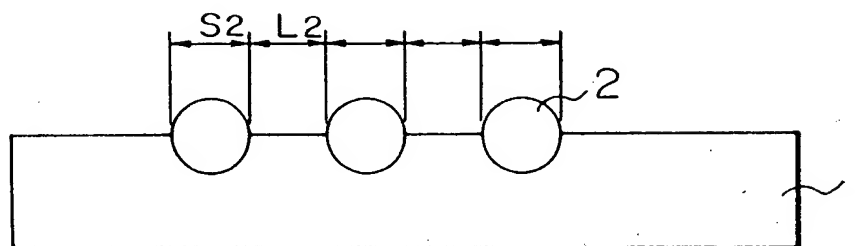
**FIG. 7**

SECTIONAL VIEW TAKEN ALONG LINE VII-VII OF FIG. 6



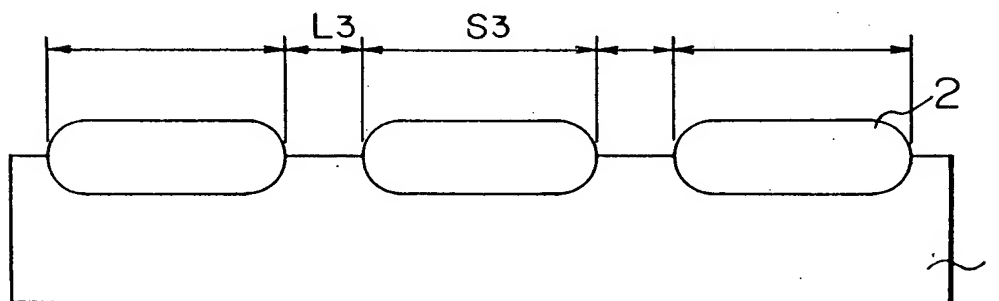
**FIG. 8**

SECTIONAL VIEW TAKEN ALONG LINE VIII-VIII OF FIG. 6



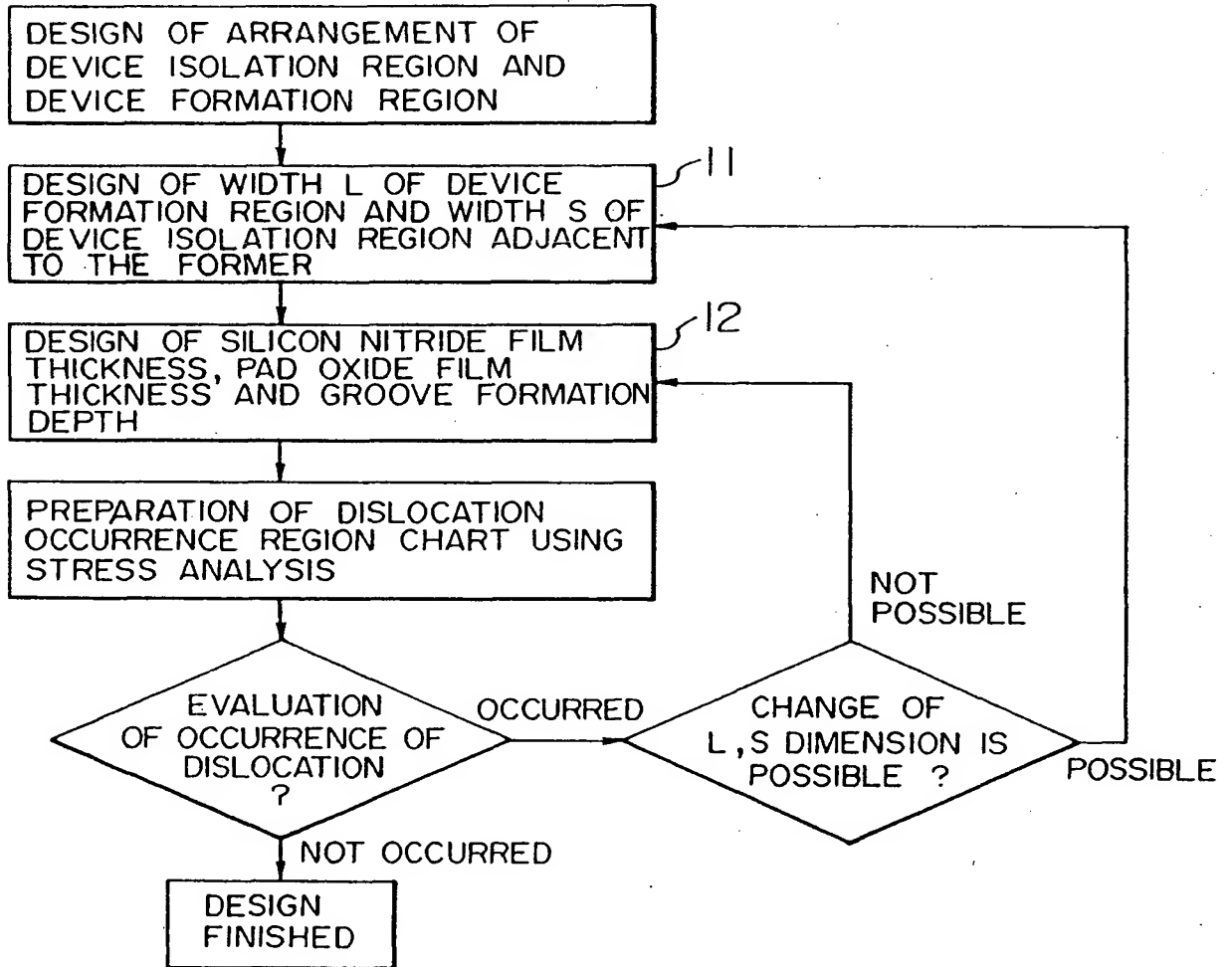
**FIG. 9**

SECTIONAL VIEW TAKEN ALONG LINE IX-IX OF FIG. 6



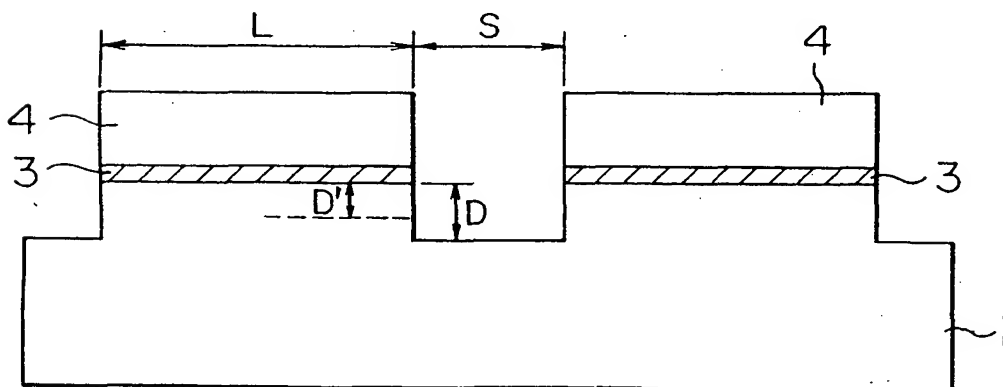
# FIG. 10

FLOW FOR DETERMINING WIDTH DIMENSION OF DEVICE FORMATION REGION OR DEVICE ISOLATION REGION



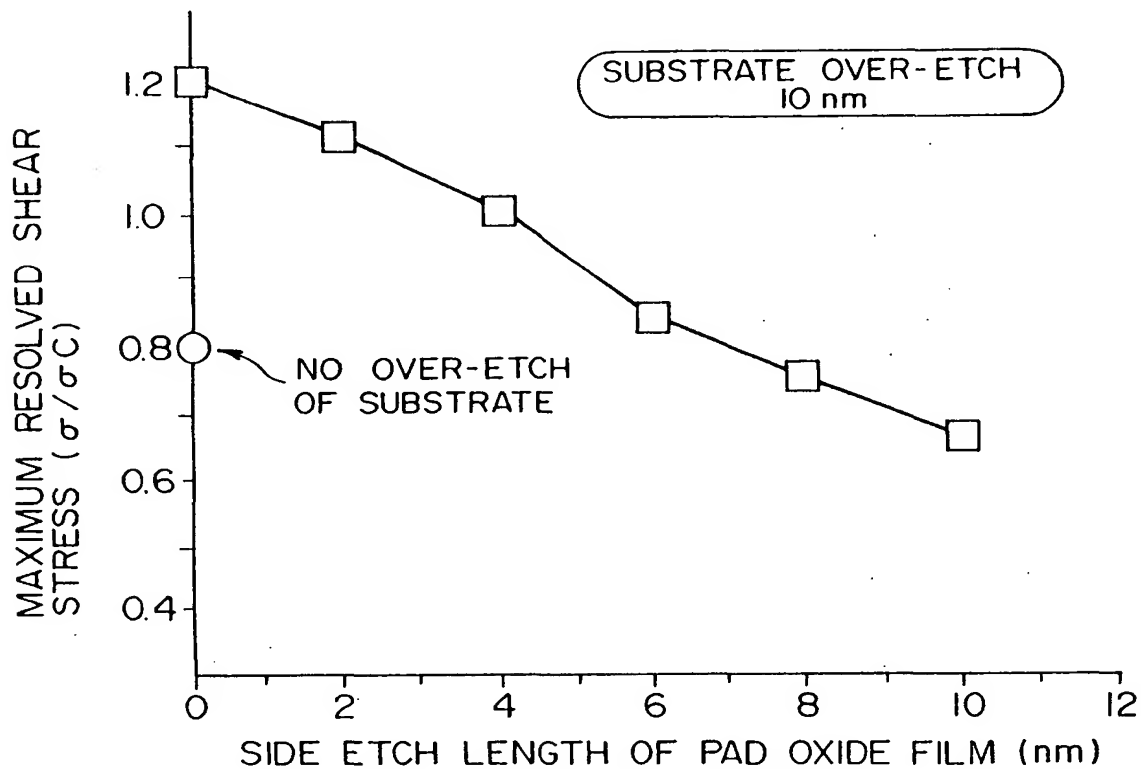
# FIG. 11

SECTIONAL VIEW OF SEMICONDUCTOR DEVICE AFTER GROOVE FORMATION



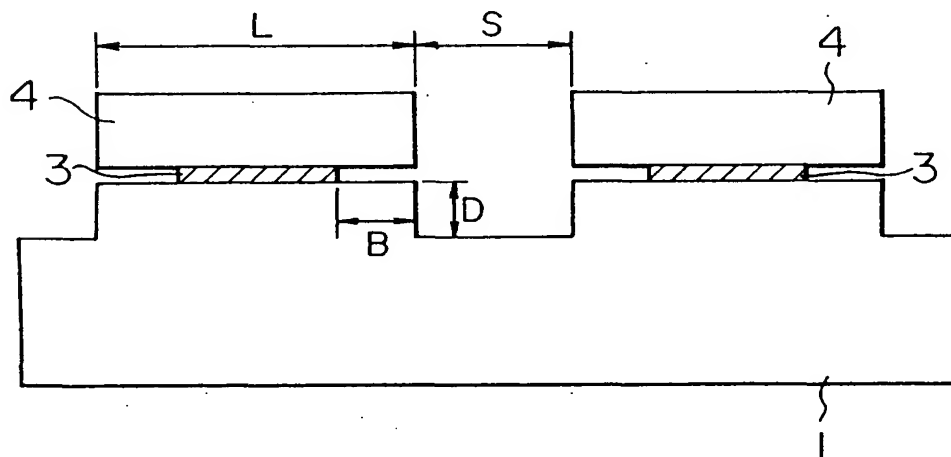
# FIG. 12

RELATION BETWEEN ETCH-BACK DISTANCE OF PAD OXIDE FILM AND MAXIMUM STRESS NEAR GROOVE END



# FIG. 13

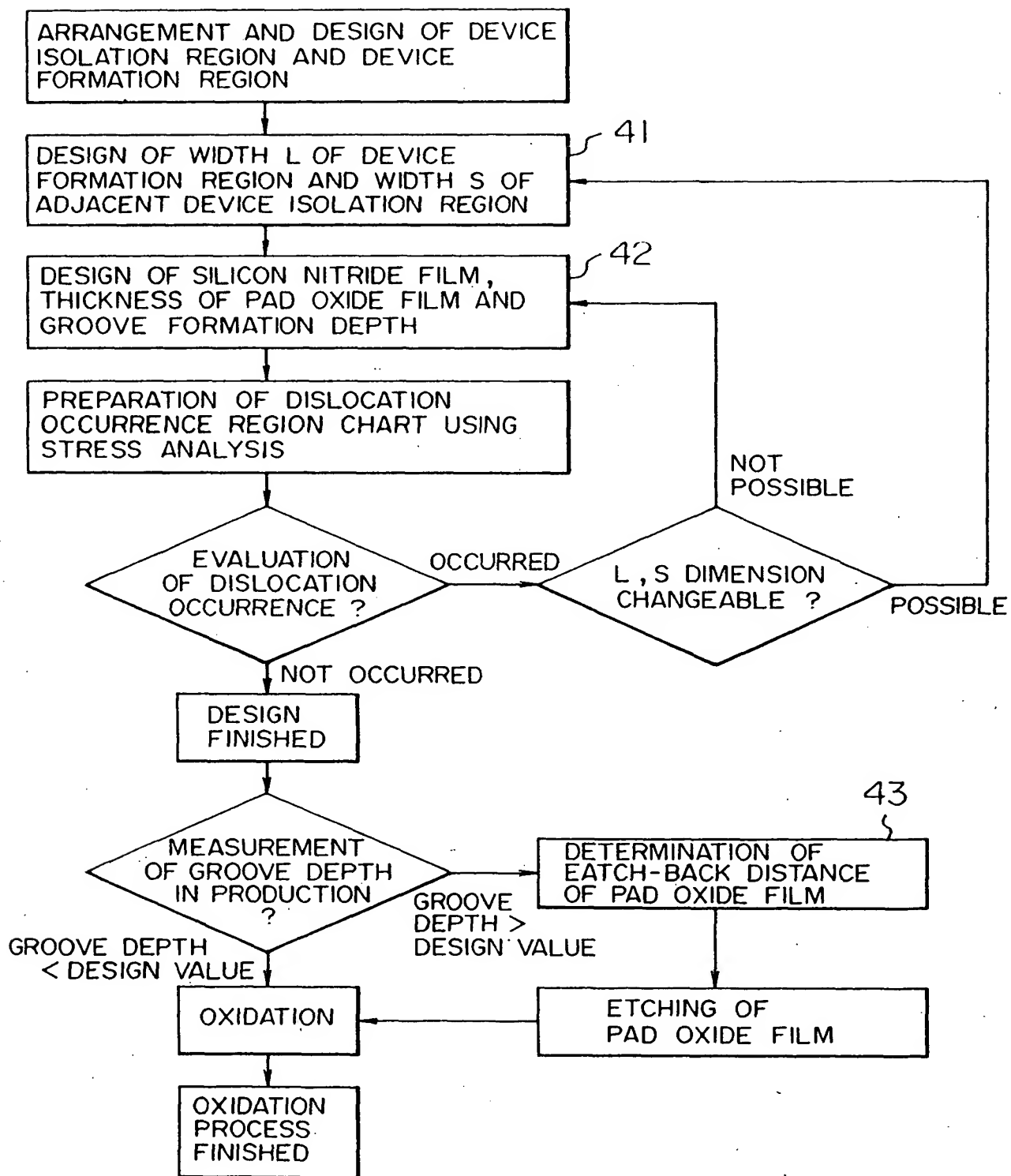
SECTION OF DEVICE AFTER ETCH-BACK OF PAD OXIDE FILM





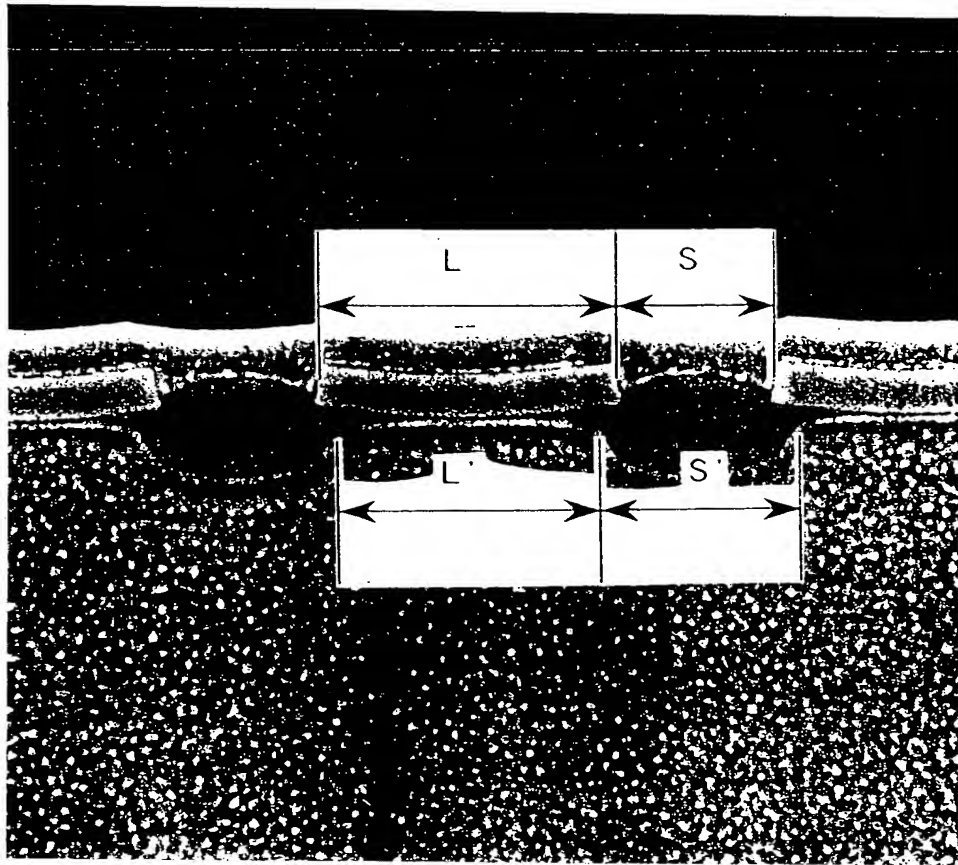
# FIG. 14

FLOW FOR DETERMINING WIDTH OF DEVICE FORMATION REGION  
OR DEVICE ISOLATION REGION

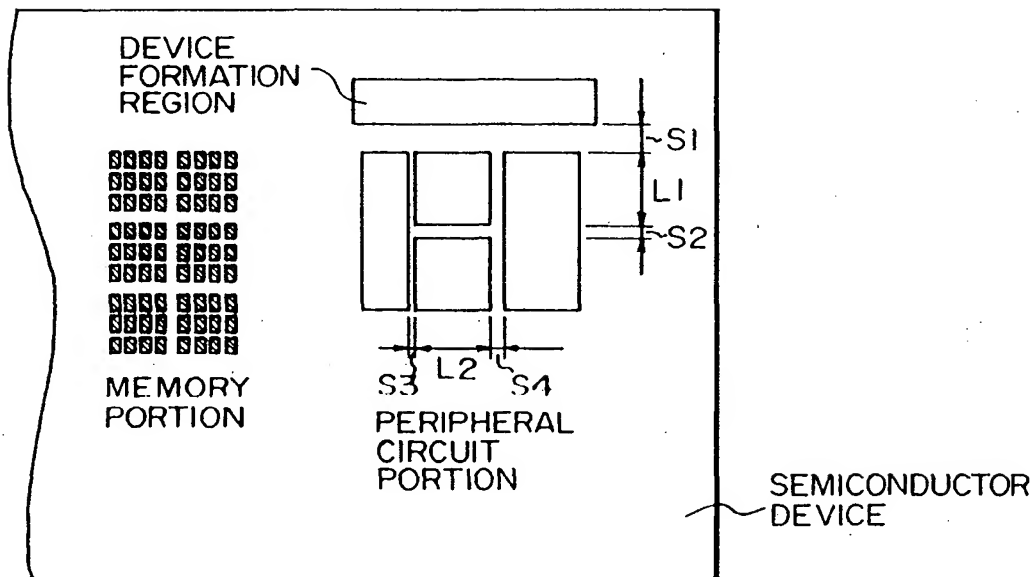


# F I G. 15

MICROGRAPH OF SEMICONDUCTOR CRYSTAL STRUCTURE SHOWING FORMATION  
EXAMPLE OF DEVICE ISOLATION REGION



# FIG. 16



# FIG. 17

## STRESS ANALYSIS STEP

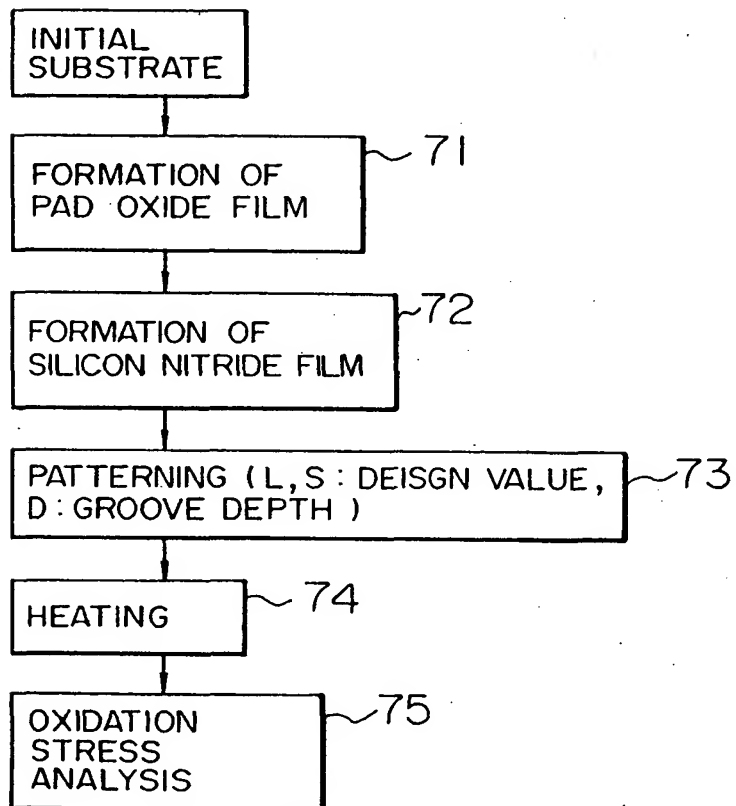
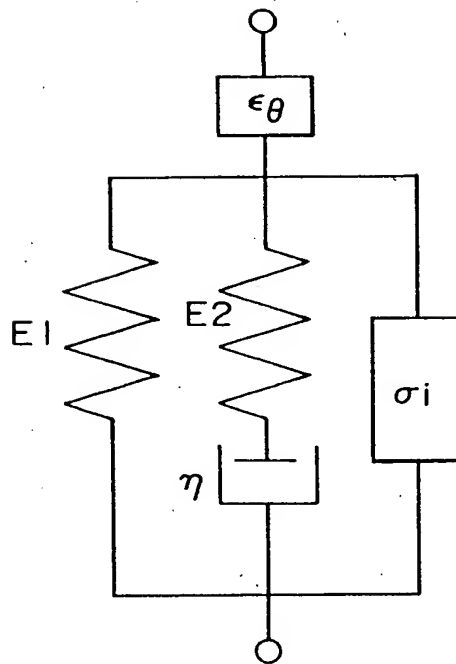


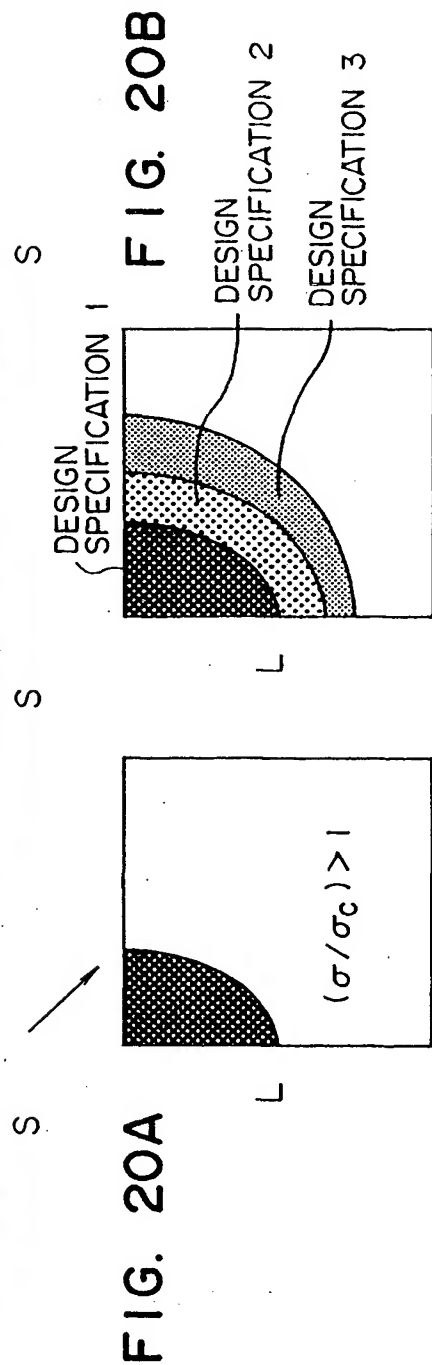
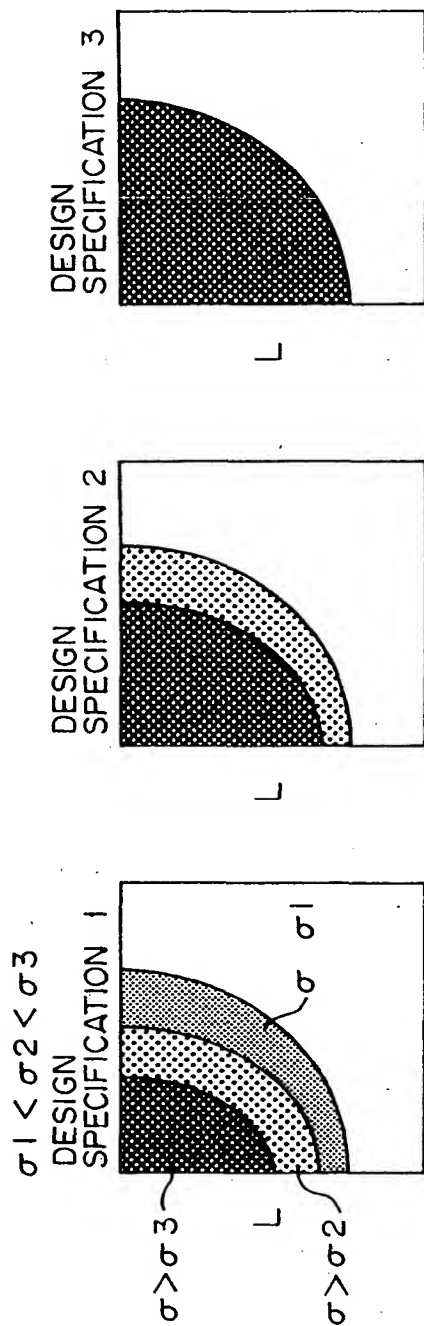
FIG. 18



VISCO-ELASTIC MODEL FOR STRESS ANALYSIS

STRESS DISTRIBUTION CHART OF EACH SPECIFICATION

FIG. 19A      FIG. 19B      FIG. 19C



DESIGN CHART OF  
DESIGN SPECIFICATION 1

DOT REGION:  $(\sigma/\sigma_c) > 1$

COLLECTIVE  
DESIGN CHART

FIG. 21

